UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/602,369 | 06/24/2003 | Michael W. Dotson | END920030008US1 | 1172 |

23550 7590 06/28/2005

HOFFMAN WARNICK & D'ALESSANDRO, LLC
3 E-COMM SQUARE
ALBANY, NY 12207

| EXAMINER | |
|---|---|
| TO, TUYEN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/602,369 | DOTSON ET AL. | |
| | Examiner | Art Unit | |
| | Tuyen To | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06/24/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/24/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This is a response to the communication filed on the 06/24/2003. Claims 1-22 are pending.

### *Specification*

The disclosure is objected to because of the following informalities: on page 12 [0028] the number 58 in the " corrective action system 58" appears to be an error because the " corrective action system" was shown with the number 56 in the drawing (Fig. 3). Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

*(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

**Claims 1-22 are rejected** under 35 U.S.C. 102(e) as being anticipated by Chui et al. (Chui) (US Patent No. 6584606 B1).

The applied reference has a common assignee (IBM corporation) with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

**Referring to claim 1**, Chui discloses the system for positioning I/0 pads (Fig. 1) on a chip, comprising:

an information access system for accessing a control file that includes a proposed placement of a set of I/0 pad groups on the chip (*Fig.1*; *col. 6 lines 16-24*);

a calculation system for calculating ( *Fig. 1; col.6, lines 51+*) a group switching current of a particular I/0 pad group identified in the control file based on individual switching currents of each I/0 pad in the particular I/0 each group (*Table 1,col. 6, lines 12-15; col. 9, lines 40-59 electromigration analysis inherently incorporates calculating switching currents both individual and group*), and for comparing the group switching current to a predetermined maximum switching current ( *Table 1; Fig. 1; col. 6, lines 51+* ); and

a corrective action system for implementing a corrective action if the group switching current exceeds the predetermined maximum switching current (Fig. 1; *col. 7, lines 14-25; col.8, lines 1-13*).

**Referring to claim 2,** Chui discloses all the limitations in claim 1, wherein the corrective action system (*see Fig.1*) relocates at least one I/0 pad in the particular I/0 pad group to another I/O pad group if the group switching current exceeds the predetermined maximum switching current (col. *7, lines 14+;* col. *8, lines 1-23*).

**Referring to claim 3,** Chui discloses all the limitations in claim 1, wherein each of the set of I/0 pad groups includes at least one power pad (*col. 1, lines 31-47*).

**Referring to claim 4,** Chui discloses all the limitations in claim 3, wherein the corrective action system inserts an additional power pad into the particular I/O pad group if the group switching current exceeds the predetermined maximum switching current (*col.7, line 14 to col. 8 line 23*).

**Referring to claim 5,** Chui discloses all the limitations in claim 1, wherein the individual switching currents are determined from an I/O limit table (*col.6, lines 46-50*), and wherein the maximum switching current is determined from an information file (*col. 6, lines 51+*).

**Referring to claim 6,** Chui discloses all the limitations in claim 1, wherein the chip is a peripheral wire bond chip (col. *1, line 38-47; col. 5, lines 56-60; col. 7, lines 9-13*).

**Referring to claim 7,** Chui discloses all the limitations in claim 1, further comprising an error detection system for detecting and reporting errors in the control file ( *Fig. 1; col. 7, lines 14-35*).

**Referring to claim 8,** Chui discloses the computer-implemented method for positioning I/O pads on a chip (*Fig.1; col. 3, lines 23-27)*, comprising:

providing a control file that includes a proposed placement of a set of I/O pad groups on the chip (*Fig. 1; col. 6 lines 16-24*);

calculating ( *Fig. 1; col.6, lines 51+*) a group switching current of a particular I/O pad group identified in the control file based on individual switching currents of each 1/0 pad in the particular I/O pad group ( Table 1; *col. 6, lines 12-15; col. 9, lines 40-59; electromigration analysis inherently incorporates calculating switching currents both individual and group*);

comparing the group switching current to a predetermined maximum switching current ( *Table 1; Fig. 1; col. 6, lines 51+* ); and

and implementing a corrective action if the group switching current exceeds the predetermined maximum switching current (*Fig. 1*; *col. 7, lines 14-25; col.8, lines 1-13*).

**Referring to claim 9,** Chui discloses all the limitations in claim 8, wherein the calculating step comprises calculating a group switching current of a particular I/O pad group identified in the control file by summing individual switching currents of each I/O pad in the particular I/O pad group (*Table 1; col. 9, lines 40-59; electromigration analysis inherently incorporates calculating switching currents both individual and group*).

**Referring to claim 10**, Chui discloses the method of claim 8, wherein the implementing step comprises relocating at least one I/O pad in the particular I/O pad group to another I/O pad group if the group switching current exceeds the predetermined maximum switching current (*col. 7, line 14 to col. 8, line 23).*

**Referring to claim 11**, Chui discloses the method claim 8, wherein each of the set of I/0 pad groups includes at least one power pad (*col. 1, lines 31-47*).

**Referring to claim 12**, Chui discloses the method of claim 11, wherein the implementing step comprises inserting an additional power pad into the particular I/O pad group if the group switching current exceeds the predetermined maximum switching current (*col.7 line 14 to col.8, line 23*).

**Referring to claim 13**, Chui discloses the method of claim 8, wherein the individual switching currents are determined from an I/O limit table (*col.6, lines 46-50*), and wherein the maximum switching current is determined from an information file (*col. 6, lines 51+).*

**Referring to claim 14**, Chui discloses the method of claim 8, further comprising: detecting errors in the control file; and reporting the errors (Fig. *1; col. 7, lines 14-35*).

**Referring to claim 15**, Chui discloses the method of claim 8, wherein the chip is a peripheral wire bond chip *(*col. *1, line 38-47; col. 5, lines 56-60; col. 7, lines 9-13*).

**Referring to claim 16**, Chui discloses the program product stored on a recordable medium for positioning I/0 pads on a chip (*Fig. 1; col. 3, lines 23-27*), which when executed comprises:

program code (*col. 3, lines 23-27; col.7, lines 25-28)* for accessing a control file that includes a proposed placement of a set of I/O pad groups on the chip (*Fig.1*; *col. 6 lines 16-24* );

program code ( *Fig. 1; col. 3, lines 23-27*) for calculating ( *Fig. 1; col.6, lines 51+*) a group switching current of a particular I/O pad group (*Table 1,col. 6, lines 12-15; col. 9, lines 40-59 electromigration analysis inherently incorporates calculating switching currents both individual and group)* identified in the control file based on individual switching currents of each I/O pad in the particular I/O pad group, and for comparing the group switching current to a predetermined maximum switching current ( *Table 1; Fig. 1; col. 6, lines 51+* ); and

program code ( *Fig. 1; col. 3, lines 23-27*) for implementing a corrective action if the group switching current exceeds the predetermined maximum switching current (Fig. 1; *col. 7, lines 14-25; col.8, lines 1-13*).

**Referring to claim 17**, Chui discloses the program product of claim 16, wherein the program code for implementing a corrective action relocates at least one I/0 pad in the particular I/O pad group to another I/O pad group if the group switching current exceeds the predetermined maximum switching current (col. *7, lines 14+;* col. *8, lines 1-23*).

**Referring to claim 18**, Chui discloses the program product claim 16, wherein each of the set of I/O pad groups includes at least one power pad (*col. 1, lines 31-47*).

**Referring to claim 19**, Chui discloses the program product claim 18, wherein the program code for implementing a corrective action inserts an additional power pad into the particular I/0 pad group if the group switching current exceeds the predetermined maximum switching current (*col.7, line 14 to col. 8 line 23*).

**Referring to claim 20**, Chui discloses the program product claim 16, wherein the individual switching currents arc determined from an I/O limit table (*col.6, lines 46-50*), and

wherein the maximum switching current is determined from an information file (*col. 6, lines 51+).*

**Referring to claim 21**, Chui discloses the program product of claim 16, further comprising program code for detecting and reporting errors in the control file (Fig. *1; col. 7, lines 14-35*).

**Referring to claim 22**, Chui discloses the program product of claim l6, wherein the chip is a peripheral wire bond chip *(*col. *1, line 38-47; col. 5, lines 56-60; col. 7, lines 9-13*).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Buffer et al. (US Patent 6499, 134) disclose a method for assigning I/O pads in integrated circuits to improve the crosstalk and time-of-flight performance.

b) Singh et al. (US Patent 6457157) discloses a method for laying out I/O pairs on an IC die.

c) Chan et al. (US Pub. No. 2003/0033578) discloses a method for enhancing a power bus for I/O libraries in ASIC design.

d) G. Yasar et al., " I/O Cell Placement and Electrical Checking Methodology for ASICs with Peripheral I/Os", IEEE 2001, Quality Electronic Design, 2001 International Symposium on 26-28 March 2001 Page(s): 71 – 75. This paper discloses an electrical checking method to be used early in a design process to verify if the I/O placements meet placement guidelines.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
Examiner
Art Unit 2825

A. M. Thompson
Primary Examiner
Technology Center 2800